Exhibit 26

[redacted]

Target

288pin Load Reduced DIMM based on 16Gb M-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First SPEC Release	21st Sep, 2018	Target	T.Y.Lee J.Y.Bae

Table Of Contents

288pin Load Reduced DIMM based on 16Gb M-die

1. DDR4 Load Reduced DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number 2)	Density	Organization	Component Composition 1)	Number of Rank	Height
M386AAG40MMB-CVF	128GB	16Gx72	DDP 8Gx4(K4ABG045WM-MC##)*36	4	31.25mm

NOTE :
1) "##" - VF
2) VF(2933Mbps 21-21-21).
- Backward compatible to lower frequency.

2. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	
tCK(min)	1.25	1.071	0.937	0.833	0.75	0.682	ns
CAS Latency	11	13	15	17	19	21	nCK
tRCD(min)	13.75	13.92	14.06	14.16	14.25	14.32	ns
tRP(min)	13.75	13.92	14.06	14.16	14.25	14.32	ns
tRAS(min)	35	34	33	32	32	32	ns
tRC(min)	48.75	47.92	47.06	46.16	46.25	46.32	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin and 1467MHz fCK for 2933Mb/sec/pin.
- 16 Banks (4 Bank Groups)
- Programmable $\overline{CAS}$ Latency: 10,11,12,13,14,15,16,17,18,19,20,21, 22
- Programmable Additive Latency (Posted $\overline{CAS}$): 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400), 14,18 (DDR4-2666) and 16, 20 (DDR4-2933).
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
8Gx4(32Gb DDP) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Load Reduced DIMM PIN COFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1) VPP is 2.5V DC
2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4) The 5th VPP is required on all modules. DIMMs.

Target

288pin Load Reduced DIMM based on 16Gb M-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First SPEC Release	7th Jul, 2018	Target	T.Y.Lee J.Y.Bae

Table Of Contents

288pin Load Reduced DIMM based on 16Gb M-die

1. DDR4 Load Reduced DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number [2]	Density	Organization	Component Composition [1]	Number of Rank	Height
M386ABG40M50-CYF	256GB	32Gx72	3DS 4H 16Gx4 (K4ACG045WM-5C##)*36	8 (2 physical ranks / 4 logical ranks)	31.25mm

NOTE :
1) "##" - RB/TC/WD/YF
2) YF(2933Mbps 24-21-21)
- Backward compatible to lower frequency.

2. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
	17-15-15	19-17-17	22-19-19	24-21-21	
tCK(min)	0.937	0.833	0.75	0.682	ns
CAS Latency	17	19	22	24	nCK
tRCD(min)	14.06	14.16	14.25	14.32	ns
tRP(min)	14.06	14.16	14.25	14.32	ns
tRAS(min)	33	32	32	32	ns
tRC(min)	47.06	46.16	46.25	46.32	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin and 1467MHz fCK for 2933Mb/sec/pin.
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 11,12,13,14,15,16,17,18,19,20,21, 22,23,24,25
- Programmable Additive Latency (Posted CAS): 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400), 14,18 (DDR4-2666) and 16, 20 (DDR4-2933).
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
16Gx4(64Gb 3DS 4H) based Module	A0-A17	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Load Reduced DIMM PIN COFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1) VPP is 2.5V DC
2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4) The 5th VPP is required on all modules. DIMMs.

Target

288pin Load Reduced DIMM based on 16Gb M-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First SPEC Release	21st Sep, 2018	Target	T.Y.Lee J.Y.Bae

Table Of Contents

288pin Load Reduced DIMM based on 16Gb M-die

1. DDR4 Load Reduced DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number [2]	Density	Organization	Component Composition [1]	Number of Rank	Height
M386ABG40M5B-CYF	256GB	32Gx72	3DS 4H 16Gx4 (K4ACG045WM-5C##)*36	8 (2 physical ranks / 4 logical ranks)	31.25mm

NOTE :
1) "##" - RB/TC/WD/YF
2) YF(2933Mbps 24-21-21)
- Backward compatible to lower frequency.

2. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
	17-15-15	19-17-17	22-19-19	24-21-21	
tCK(min)	0.937	0.833	0.75	0.682	ns
CAS Latency	17	19	22	24	nCK
tRCD(min)	14.06	14.16	14.25	14.32	ns
tRP(min)	14.06	14.16	14.25	14.32	ns
tRAS(min)	33	32	32	32	ns
tRC(min)	47.06	46.16	46.25	46.32	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin and 1467MHz fCK for 2933Mb/sec/pin.
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 11,12,13,14,15,16,17,18,19,20,21, 22,23,24,25
- Programmable Additive Latency (Posted CAS): 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400), 14,18 (DDR4-2666) and 16, 20 (DDR4-2933).
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
16Gx4(64Gb 3DS 4H) based Module	A0-A17	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Load Reduced DIMM PIN COFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1) VPP is 2.5V DC
2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4) The 5th VPP is required on all modules. DIMMs.

Target

288pin Load Reduced DIMM based on 16Gb M-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First SPEC Release	5th Jun, 2018	Target	T.Y.Lee J.Y.Bae

Table Of Contents

288pin Load Reduced DIMM based on 16Gb M-die

1. DDR4 Load Reduced DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number 2)	Density	Organization	Component Composition 1)	Number of Rank	Height
M386AAG40MM2-CVF	128GB	16Gx72	DDP 8Gx4(K4ABG045WM-MC##)*36	4	31.25mm

NOTE :
1) "##" - VF
2) VF(2933Mbps 21-21-21).
- Backward compatible to lower frequency.

2. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	
tCK(min)	1.25	1.071	0.937	0.833	0.75	0.682	ns
CAS Latency	11	13	15	17	19	21	nCK
tRCD(min)	13.75	13.92	14.06	14.16	14.25	14.32	ns
tRP(min)	13.75	13.92	14.06	14.16	14.25	14.32	ns
tRAS(min)	35	34	33	32	32	32	ns
tRC(min)	48.75	47.92	47.06	46.16	46.25	46.32	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin and 1467MHz fCK for 2933Mb/sec/pin.
- 16 Banks (4 Bank Groups)
- Programmable $\overline{CAS}$ Latency: 10,11,12,13,14,15,16,17,18,19,20,21, 22
- Programmable Additive Latency (Posted $\overline{CAS}$): 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400), 14,18 (DDR4-2666) and 16, 20 (DDR4-2933).
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
8Gx4(32Gb DDP) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Load Reduced DIMM PIN COFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1) VPP is 2.5V DC
2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4) The 5th VPP is required on all modules. DIMMs.

5. PIN DESCRIPTION

Pin Name	Description
A0–A17[1]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2]	Register row address strobe input
CAS_n[3]	Register column address strobe input
WE_n[4]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0–SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

288pin Load Reduced DIMM based on 8Gb B-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC Release	Jul. 2015	-	J.Y.Lee
1.1	- Change of IDD value on page 25	3rd Feb. 2016	-	J.Y.Lee
	- Change of 8.1 Timing & Capacitance values (tACT) on page 9			
	- Change of Physical Dimensions (Module Thickness) on page 38			
1.2	- Update Physical dimension. 1. Add PCB hole. 2. Update Module height information. - Update Absolute Maximum Ratings. - Update Input/Output Capacitance.	8th Jun, 2017	Final	J.Y.Bae
1.3	- Update INPUT/OUTPUT FUNCTIONAL DESCRIPTION. - Update AC & DC INPUT MEASUREMENT LEVELS. - Add AC AND DC OUTPUT MEASUREMENT LEVELS. - Update TIMING PARAMETERS BY SPEED GRADE	9th Feb. 2018	Final	Hyeon. Kang J.Y.Bae

Table Of Contents

288pin Load Reduced DIMM based on 8Gb B-die

1. DDR4 Load Reduced DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number 2)	Density	Organization	Component Composition 1)	Number of Rank	Height
M386A8K40BMB-CPB/RC	64GB	8Gx72	DDP 4Gx4(K4AAG045WB-MC##)*36	4	31.25mm

NOTE :
1) "##" - PB/RC
2) PB(2133Mbps 15-15-15)/RC(2400Mbps 17-17-17)
- DDR4-2400(17-17-17) is backward compatible to DDR4-2133(15-15-15)

2. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	
tCK(min)	1.25	1.071	0.938	0.833	ns
CAS Latency	11	13	15	17	nCK
tRCD(min)	13.75	13.92	14.06	14.16	ns
tRP(min)	13.75	13.92	14.06	14.16	ns
tRAS(min)	35	34	33	32	ns
tRC(min)	48.75	47.92	47.06	46.16	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18
- Programmable Additive Latency (Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133) and 12,16 (DDR4-2400)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
4Gx4(16Gb DDP) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Load Reduced DIMM PIN CONFIGURATIONS (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE :

1) VPP is 2.5V DC.
2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM.
4) The 5th VPP is required on all modules. DIMMs.

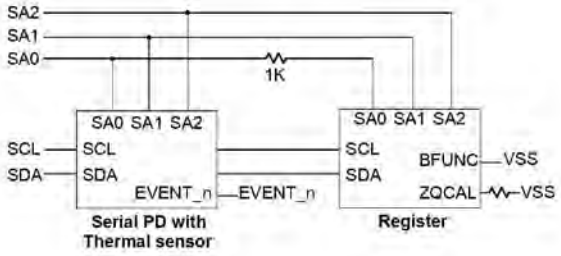
5. PIN DESCRIPTION

Pin Name	Description
A0-A17[1]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2]	Register row address strobe input
CAS_n[3]	Register column address strobe input
WE_n[4]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0-CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c-DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0-SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

6. ON DIMM THERMAL SENSOR



NOTE :
1) All Samsung RDIMM support Thermal sensor on DIMM.

[Table 3] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

288pin Load Reduced DIMM based on 8Gb C-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC Release	7th Apr. 2017	-	J.Y.Lee
1.1	- Update Physical Dimension. 1. Add PCB hole. 2. Change Module height information.	13th Jun. 2017	Final	J.Y.Bae
1.2	- Add 2933Mbps. - Correct typo.	6th Feb. 2018	Final	J.H.Han J.Y.Bae

Table Of Contents

288pin Load Reduced DIMM based on 8Gb C-die

1. DDR4 Load Reduced DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number 2)	Density	Organization	Component Composition 1)	Number of Rank	Height
M386A8K40CM2-CRC/TD/VF	64GB	8Gx72	DDP 4Gx4(K4AAG045WC-MC##)*36	4	31.25mm

NOTE :
1) "##" - RC/TD/VF
2) RC(2400Mbps 17-17-17)/TD(2666Mbps 19-19-19)/VF(2933Mbps 21-21-21).
- Backward compatible to lower frequency.

2. KEY FEATURES

[Table 2] Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	
tCK(min)	1.25	1.071	0.937	0.833	0.75	0.682	ns
CAS Latency	11	13	15	17	19	21	nCK
tRCD(min)	13.75	13.92	14.06	14.16	14.25	14.32	ns
tRP(min)	13.75	13.92	14.06	14.16	14.25	14.32	ns
tRAS(min)	35	34	33	32	32	32	ns
tRC(min)	48.75	47.92	47.06	46.16	46.25	46.32	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin and 1467MHz fCK for 2933Mb/sec/pin.
- 16 Banks (4 Bank Groups)
- Programmable $\overline{CAS}$ Latency: 10,11,12,13,14,15,16,17,18,19,20,21
- Programmable Additive Latency (Posted $\overline{CAS}$): 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400), 14,18 (DDR4-2666) and 16, 20 (DDR4-2933).
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
4Gx4(16Gb DDP) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

4. Load Reduced DIMM PIN COFIGURATIONS (FRONT SIDE / BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1) VPP is 2.5V DC
2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4) The 5th VPP is required on all modules. DIMMs.

5. PIN DESCRIPTION

Pin Name	Description
A0–A17[1]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2]	Register row address strobe input
CAS_n[3]	Register column address strobe input
WE_n[4]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0–SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.